Integrated Silicon Pressure Sensor On-Chip Signal Conditioned, Temperature Compensated, and Calibrated

The MPX5100 series piezoresistive transducer is a state-of-the-art monolithic silicon pressure sensor designed for a wide range of applications, but particularly those employing a microcontroller or microprocessor with A/D inputs. This patented, single element transducer combines advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high level analog output signal that is proportional to the applied pressure.

Features

- 2.5% Maximum Error over 0° to 85°C
- Ideally suited for Microprocessor or Microcontroller-Based Systems
- Patented Silicon Shear Stress Strain Gauge
- Available in Absolute, Differential and Gauge Configurations
- Durable Epoxy Unibody Element
- Easy-to-Use Chip Carrier Option

Typical Applications

- Patient Monitoring
- Process Control
- Pump/Motor Control
- Pressure Switching

ORDERING INFORMATION						
Device Type	Options	Case No.	MPX Series Order Number	Device Marking		
UNIBODY	PACKAGE (MPX5100 SE	ERIES)				
Basic	Absolute	867	MPX5100A	MPX5100A		
Elements	Differential	867	MPX5100D	MPX5100D		
Ported	Differential Dual Ports	867C	MPX5100DP	MPX5100DP		
Elements	Absolute, Single Port	867B	MPX5100AP	MPX5100AP		
	Gauge, Single Port	867B	MPX5100GP	MPX5100GP		
	Gauge, Axial PC Mount	867F	MPX5100GSX	MPX5100D		
	Gauge, Axial Port, SMT	482A	MPXV5100GC6U	MPXV5100G		
	Gauge, Axial Port, DIP	482C	MPX5V100GC7U	MPXV5100G		
	Gauge, Dual Port, SMT	1351	MPXV5100DP	MPXV5100		
	Gauge, Side Port, SMT	1369	MPXV5100GP	MPXV5100G		

MPX5100/MPXV5100 SERIES

INTEGRATED PRESSURE SENSOR 0 to 100 kpa (0 to 14.5 psi) 15 to 115 kPa (2.2 to 16.7 psi) 0.2 to 4.7 V Output

SMALL OUTLINE PACKAGES





MPXV5100GC6U CASE 482A-01

MPXV5100GC7U CASE 482C-03





MPXV5100DP CASE 1351-01

MPXV5100GP CASE 1369-01

PIN NUMBER ⁽¹⁾						
1	N/C	5	N/C			
2	٧s	6	N/C			
3	GND	7	N/C			
4	V _{OUT}	8	N/C			

 Pins 1, 5, 6, 7, and 8 are internal device connections. Do not connect to external circuitry or ground. Pin1 is noted by the notch in the lead.

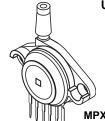
PIN NUMBER ⁽¹⁾					
1	V _{OUT}	4	N/C		
2	GND	5	N/C		
3	٧s	6	N/C		

 Pins 4, 5, and 6 are internal device connections. Do not connect to external circuitry or ground. Pin 1 is noted by the notch in the lead.





MPX5100A/D CASE 867-08



MPX5100AP/GP CASE 867B-04





MPX5100GSX CASE 867F-03



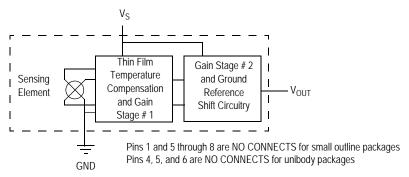


Figure 1. Fully Integrated Pressure Sensor Schematic

TABLE 1. Maximum Ratings⁽¹⁾

Rating	Symbol	Value	Unit
Maximum Pressure (P1 > P2)	P _{MAX}	400	kPa
Storage Temperature	T _{STG}	-40° to +125°C	°C
Operating Temperature	T _A	-40° to +125°C	°C

^{1.} Exposure beyond the specified limits may cause permanent damage or degradation to the device.

TABLE 2. Operating Characteristics ($V_S = 5.0 V_{DC}$, $T_A = 25^{\circ}C$ unless otherwise noted, P1 > P2. Decoupling circuit shown in Figure 4 required to meet electrical specifications.)

Characteristic	Symbol	Min	Тур	Max	Unit
Pressure Range ⁽¹⁾ Gauge, Differential: MPX5100D/MPX5100G/MPXV5100G Absolute: MPX5100A	P _{OP}	0 15		100 115	kPa
Supply Voltage ⁽²⁾	V _S	4.75	5.0	5.25	V _{DC}
Supply Current	Io	_	7.0	10	mAdc
Minimum Pressure Offset ⁽³⁾ (0 to 85°C) @ $V_S = 5.0 \text{ V}$	V _{OFF}	0.088	0.20	0.313	V _{DC}
Full Scale Output ⁽⁴⁾ Differential and Absolute (0 to 85°C) @ V _S = 5.0 V	V _{FSO}	4.587	4.700	4.813	V _{DC}
Full Scale Span ⁽⁵⁾ Differential and Absolute (0 to 85°C) @ V _S = 5.0 V	V _{FSS}	_	4.500	_	V _{DC}
Accuracy ⁽⁶⁾	_	_	_	±2.5	%V _{FSS}
Sensitivity	V/P	_	45	_	mV/kPa
Response Time ⁽⁷⁾	t _R	_	1.0	_	ms
Output Source Current at Full Scale Output	I _{O+}	_	0.1	_	mAdc
Warm-Up Time ⁽⁸⁾	_	_	20	_	ms
Offset Stability ⁽⁹⁾	_	_	±0.5	_	%V _{FSS}

- 1. 1 kPa (kiloPascal) equals 0.145 psi.
- 2. Device is ratiometric within this specified excitation range.
- 3. Offset (V_{OFF}) is defined as the output voltage at the minimum rated pressure.
- 4. Full Scale Output (V_{FSO}) is defined as the output voltage at the maximum or full rated pressure.
- Full Scale Span (V_{FSS}) is defined as the algebraic difference between the output voltage at full rated pressure and the output voltage at the minimum rated pressure.
- 6. Accuracy (error budget) consists of the following:
 - Linearity: Output deviation from a straight line relationship with pressure over the specified pressure range.
 - Temperature Hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to
 - and from the minimum or maximum operating temperature points, with zero differential pressure applied.
 - Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from minimum or maximum rated pressure at 25°C.
 - TcSpan: Output deviation over the temperature range of 0° to 85°C, relative to 25°C.
 - TcOffset: Output deviation with minimum pressure applied over the temperature range of 0° to 85°C, relative to 25°C.
 - Variation from Nominal: The variation from nominal values, for Offset or Full Scale Span, as a percent of V_{FSS} at 25°C.

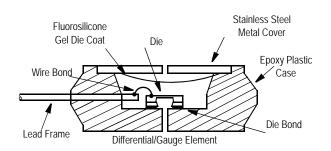
- 7. Response Time is defined as the time for the incremental changed in the output to go from 10% to 90% of its final value when subjected to a specified step change in pressure.
- 8. Warm-Up Time is defined as the time required for the product to meet the specified output voltage after the Pressure has been stabilized.
- 9. Offset Stability is the product's output deviation when subjected to 1000 hours of Pulsed Pressure, Temperature Cycling with Bias Test.

ON-CHIP TEMPERATURE COMPENSATION, CALIBRATION AND SIGNAL CONDITIONING

Figure 2 shows the sensor output signal relative to pressure input. Typical, minimum, and maximum output curves are shown for operation over a temperature range of 0x to 85xC using the decoupling circuit shown in Figure 4. The output will saturate outside of the specified pressure range.

Figure 3 illustrates both the Differential/Gauge and the Absolute Sensing Chip in the basic chip carrier (Case 867). A fluorosilicone gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the sensor diaphragm.

The MPX5100 series pressure sensor operating characteristics, and internal reliability and qualification tests are based on use of dry air as the pressure media. Media, other than dry air, may have adverse effects on sensor performance and long-term reliability. Contact the factory for information regarding media compatibility in your application.



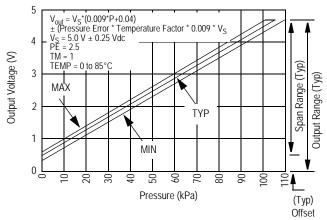


Figure 2. Output Vs. Pressure Differential

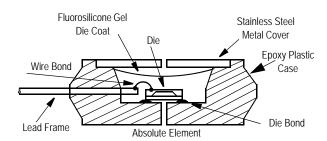


Figure 3. Cross Sectional Diagrams (Not to Scale)

Figure 4 shows the recommended decoupling circuit for interfacing the output of the integrated sensor to the A/D input

of a microprocessor or microcontroller. Proper decoupling of the power supply is recommended.

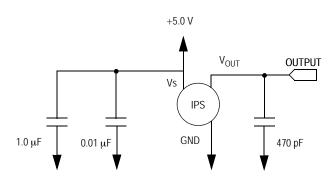


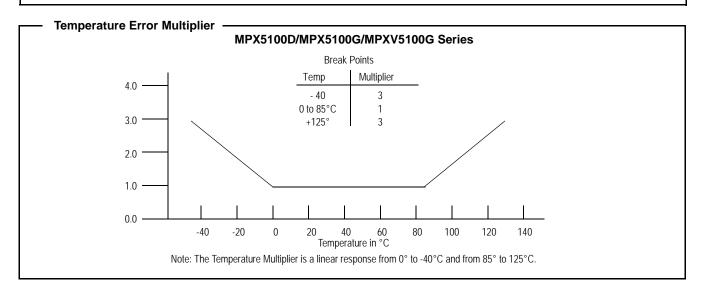
Figure 4. Recommended Power Supply Decoupling and Output Filtering (For additional output filtering, please refer to Application Note AN1646.)

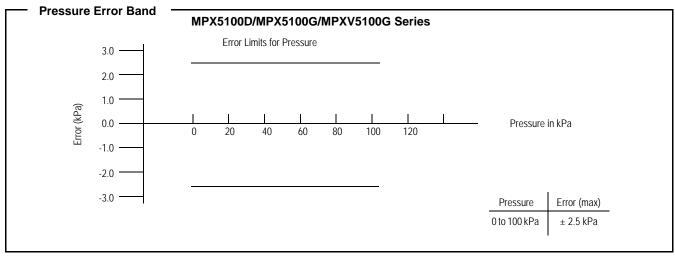
Transfer Function (MPX5100D, MPX5100G, MPXV5100G

Nominal Transfer Value: $V_{OUT} = V_S (P \times 0.009 + 0.04)$

 \pm (Pressure Error x Temp. Mult. x 0.009 x $V_S)$

 $V_S = 5.0 V \pm 5\% P kPa$



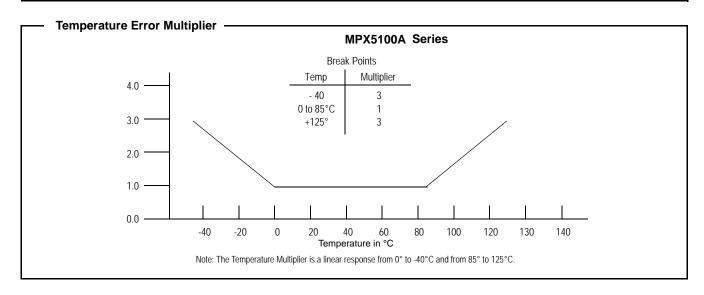


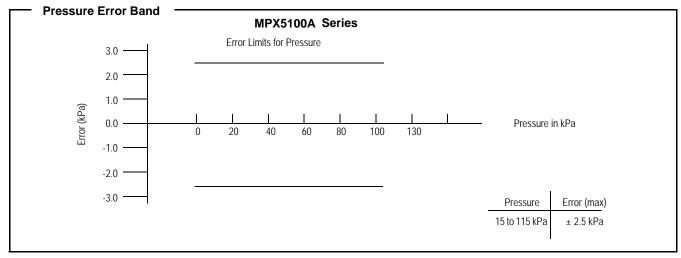
Transfer Function (MPX5100A) —

Nominal Transfer Value: $V_{OUT} = V_S (P \times 0.009 - 0.095)$

 \pm (Pressure Error x Temp. Mult. x 0.009 x $V_S)$

 $V_S = 5.0 V \pm 5\% P kPa$





PRESSURE (P1)/VACUUM (P2) SIDE IDENTIFICATION TABLE

Freescale designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The Pressure (P1) side is the side containing fluoro silicone gel which protects the die from harsh media. The MPX pressure

sensor is designed to operate with positive differential pressure applied, P1 > P2.

The Pressure (P1) side may be identified by using Table 3 below.

TABLE 3. PRESSURE (P1)/VACUUM (P2) SIDE IDENTIFICATION TABLE

Part Number	Case Type	Pressure (P1) Side Identifier
MPX5100A, MPX5100D	867	Stainless Steel Cap
MPX5100DP	867C	Side with Part Marking
MPX5100AP, MPX5100GP	867B	Side with Port Attached
MPX5100GSX	867F	Side with Port Attached
MPXV5100GC6U	482A	Side with Port Attached
MPXV5100GC7U	482C	Side with Port Attached
MPXV5100DP	1351	Side with Part Marking
MPXV5100GP	1369	Side with Port Attached

INFORMATION FOR USING THE SMALL OUTLINE PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct

footprint, the packages will self align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder

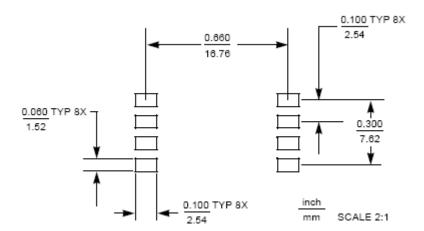
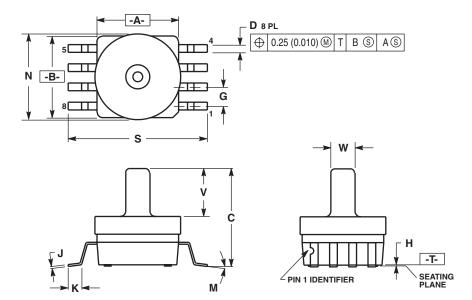


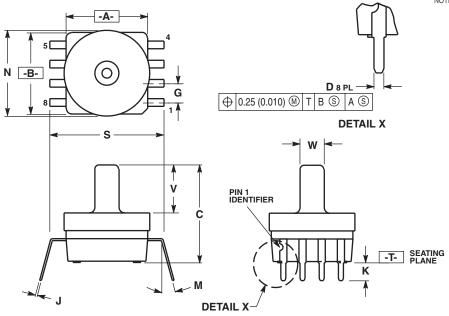
Figure 5. Small Outline Package Footprint



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
 5. ALL VERTICAL SURFACES 5' TYPICAL DRAFT.

	INCHES		MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.415	0.425	10.54	10.79
В	0.415	0.425	10.54	10.79
С	0.500	0.520	12.70	13.21
D	0.038	0.042	0.96	1.07
G	0.100	BSC	2.54 BSC	
Н	0.002	0.010	0.05	0.25
J	0.009	0.011	0.23	0.28
K	0.061	0.071	1.55	1.80
M	0°	7°	0°	7°
N	0.444	0.448	11.28	11.38
S	0.709	0.725	18.01	18.41
٧	0.245	0.255	6.22	6.48
W	0.115	0.125	2.92	3.17

CASE 482A-01 ISSUE A SMALL OUTLINE PACKAGE



CASE 482C-03 ISSUE B SMALL OUTLINE PACKAGE

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

- 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.

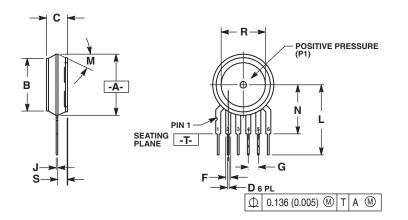
- MOLD PHO I HUSION.

 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).

 5. ALL VERTICAL SURFACES 5" TYPICAL DRAFT.

 6. DIMENSION S TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INC	HES	MILLIMETER		
DIM	MIN	MAX	MIN	MAX	
Α	0.415	0.425	10.54	10.79	
В	0.415	0.425	10.54	10.79	
С	0.500	0.520	12.70	13.21	
D	0.026	0.034	0.66	0.864	
G	0.100	BSC	2.54 BSC		
J	0.009	0.011	0.23	0.28	
K	0.100	0.120	2.54	3.05	
M	0°	15°	0°	15°	
N	0.444	0.448	11.28	11.38	
S	0.540	0.560	13.72	14.22	
٧	0.245	0.255	6.22	6.48	
W	0.115	0.125	2.92	3.17	



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION -A- IS INCLUSIVE OF THE MOLD STOP RING, MOLD STOP RING NOT TO EXCEED 16.00 (1952). 16.00 (0.630).

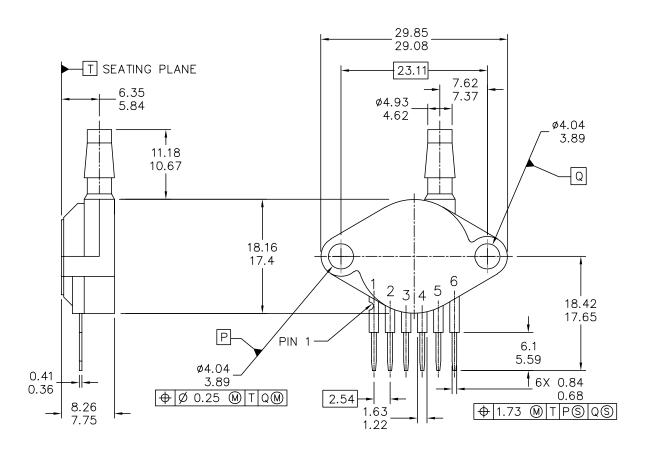
	INCHES		MILLIM	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.595	0.630	15.11	16.00
В	0.514	0.534	13.06	13.56
С	0.200	0.220	5.08	5.59
D	0.027	0.033	0.68	0.84
F	0.048	0.064	1.22	1.63
G	0.100	BSC	2.54	BSC
J	0.014	0.016	0.36	0.40
L	0.695	0.725	17.65	18.42
M	30° l	MOV	30° NOM	
N	0.475	0.495	12.07	12.57
R	0.430	0.450	10.92	11.43
S	0.090	0.105	2.29	2.66

VOUT
GROUND
VCC
V1
V2
VEX

STYLE 2: PIN 1. OPEN 2. GROUND 3. -VOUT 4. VSUPPLY 5. +VOUT 6. OPEN

STYLE 3:
PIN 1. OPEN
2. GROUND
3. +VOUT
4. +VSUPPLY
5. -VOUT
6. OPEN

CASE 867-08 ISSUE N UNIBODY PACKAGE



FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICA	L OUTLINE	PRINT VERSION NO	TO SCALE
TITLE:		DOCUMENT NO	1: 98ASB42796B	REV: G
SENSOR, 6 LEAD UNIBO	CASE NUMBER: 867B-04 28 JUL 200			
AP & GP 01ASB09087B		STANDARD: NO	IN-JEDEC	

PAGE 1 OF 2

CASE 867B-04 ISSUE G UNIBODY PACKAGE

NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- 3. 867B-01 THRU -3 OBSOLETE, NEW STANDARD 867B-04.

STYLE 1:

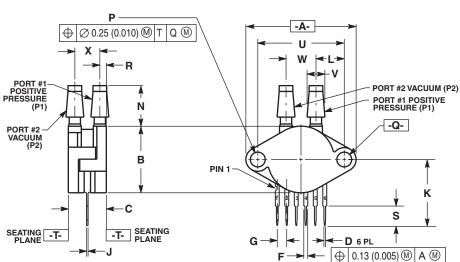
PIN 1: V OUT

2: GROUND 3: VCC 4: V1 5: V2 6: V EX

	MECHANICA	L OUTLINE	PRINT VERSION NO	T TO SCALE
TITLE:	DOCUMENT NO): 98ASB42796B	REV: G	
SENSOR, 6 LEAD UNIBO	CASE NUMBER: 867B-04 28 JUL 200			
AP & GP 01ASB09087B		STANDARD: NO	DN-JEDEC	

PAGE 2 OF 2

CASE 867B-04 ISSUE G UNIBODY PACKAGE



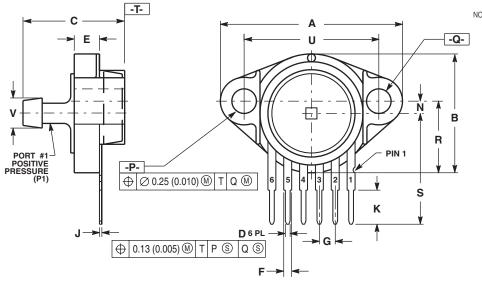
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: INCH.

	INC	HES	MILLIMETERS			
DIM	MIN	MAX	MIN	MAX		
Α	1.145	1.175	29.08	29.85		
В	0.685	0.715	17.40	18.16		
С	0.405	0.435	10.29	11.05		
D	0.027	0.033	0.68	0.84		
F	0.048	0.064	1.22	1.63		
G	0.100	BSC	2.54 BSC			
J	0.014	0.016	0.36	0.41		
K	0.695	0.725	17.65	18.42		
L	0.290	0.300	7.37	7.62		
N	0.420	0.440	10.67	11.18		
Р	0.153	0.159	3.89	4.04		
Q	0.153	0.159	3.89	4.04		
R	0.063	0.083	1.60	2.11		
S	0.220	0.240	5.59	6.10		
U	0.910 BSC		23.11 BSC			
٧	0.182	0.194	4.62	4.93		
W	0.310	0.330	7.87	8.38		
Х	0.248	0.278	6.30	7.06		

STYLE 1:
PIN 1. Vout
2. GROUND
3. Vcc
4. V1
5. V2
6. Vex

CASE 867C-05 ISSUE F UNIBODY PACKAGE

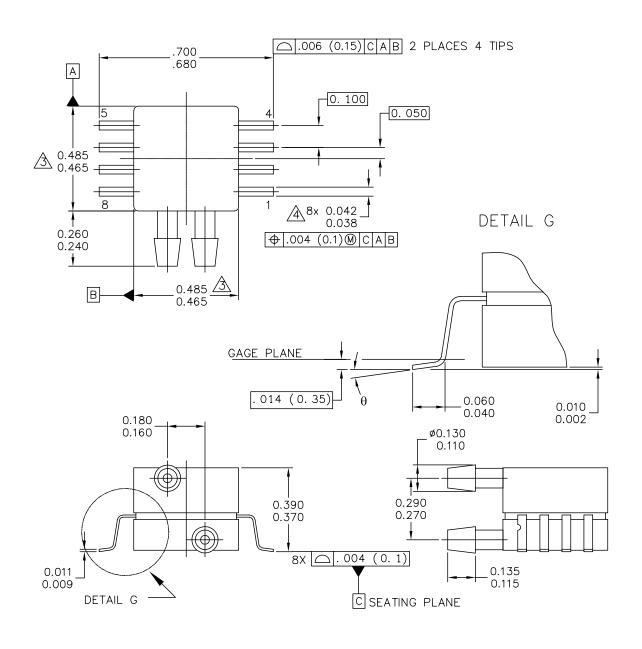


- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: INCH.

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	1.080	1.120	27.43	28.45	
В	0.740	0.760	18.80	19.30	
С	0.630	0.650	16.00	16.51	
D	0.027	0.033	0.68	0.84	
Е	0.160	0.180	4.06	4.57	
F	0.048	0.064	1.22	1.63	
G	0.100	BSC	2.54 BSC		
J	0.014	0.016	0.36	0.41	
K	0.220	0.240	5.59	6.10	
N	0.070	0.080	1.78	2.03	
Р	0.150	0.160	3.81	4.06	
Q	0.150	0.160	3.81	4.06	
R	0.440	0.460	11.18	11.68	
S	0.695	0.725	17.65	18.42	
U	0.840	0.860	21.34	21.84	
٧	0.182	0.194	4.62	4.93	

STYLE 1: PIN 1. Vout 2. GROUND 3. Vcc 4. V1 5. V2 6. Vex

CASE 867F-03 ISSUE D UNIBODY PACKAGE



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE:		DOCUMENT NO): 98ASA99255D	REV: A
8 LD SNSR, DUAL	PORT	CASE NUMBER	R: 1351–01	27 JUL 2005
		STANDARD: NO	N-JEDEC	

PAGE 1 OF 2

CASE 1351-01 ISSUE A SMALL OUTLINE PACKAGE

NOTES:

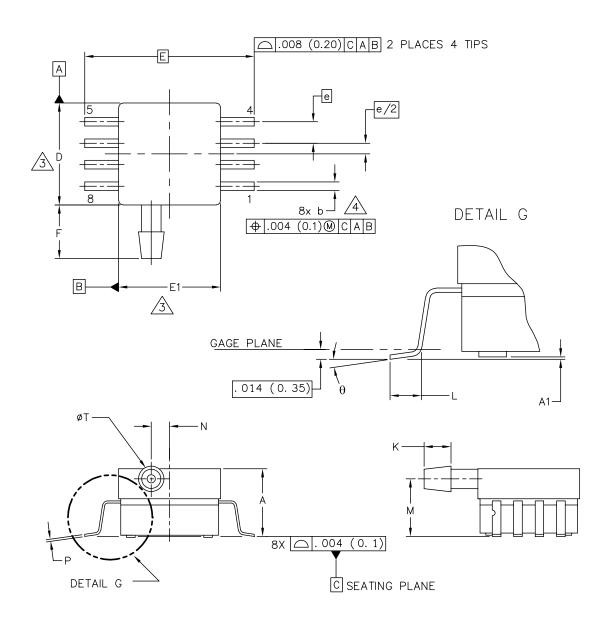
- 1. CONTROLLING DIMENSION: INCH
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS. MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE.
- DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 MAXIMUM.

STYLE 1:		STYLE 2:	
PIN 1:	GND	PIN 1:	N/C
PIN 2:	+Vout	PIN 2:	٧s
PIN 3:	٧s	PIN 3:	GND
PIN 4:	-Vout	PIN 4:	Vout
PIN 5:	N/C	PIN 5:	N/C
PIN 6:	N/C	PIN 6:	N/C
PIN 7:	N/C	PIN 7:	N/C
PIN 8:	N/C	PIN 8:	N/C

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE:		DOCUMENT NO): 98ASA99255D	REV: A
8 LD SNSR, DUAL	PORT	CASE NUMBER	R: 1351–01	27 JUL 2005
		STANDARD: NO	N-JEDEC	

PAGE 2 OF 2

CASE 1351-01 ISSUE A SMALL OUTLINE PACKAGE



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLIN	E PRINT VERSION N	PRINT VERSION NOT TO SCALE		
TITLE:	DOCUMEN	T NO: 98ASA99303D	REV: B		
8 LD SOP, SIDE PO	ORT CASE NU	CASE NUMBER: 1369-01 24 MAY 2009			
,	STANDAR	D: NON-JEDEC	•		

PAGE 1 OF 2

CASE 1369-01 ISSUE B SMALL OUTLINE PACKAGE

NOTES:

- 1. CONTROLLING DIMENSION: INCH
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
- △ DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PPROTRUSIONS.

 MOLD FLASH AND PROTRUSIONS SHALL NOT EXCEED .006 (0.152) PER SIDE.
- DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .008 (0.203) MAXIMUM.

	INCHES		MILLIMETERS			INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
Α	. 300	. 330	7. 11	7. 62	θ	0.	7 °	0,	7°
A 1	. 002	. 010	0. 05	0. 25	_				
b	. 038	. 042	0. 96	1. 07	_				
D	. 465	. 485	11. 81	12. 32	_				
E	. 717	BSC	18	. 21 BSC	_				
E1	. 465	. 485	11. 81	12. 32	_				
e	. 100	BSC	2.	54 BSC	-				
F	. 245	. 255	6. 22	6. 47	_				
K	. 120	. 130	3. 05	3. 30	_				
L	. 061	. 071	1. 55	1. 80	_				
M	. 270	. 290	6. 86	7. 36	_				
N	. 080	. 090	2. 03	2. 28	_				
Р	. 009	. 011	0. 23	0. 28	_				
Т	. 115	. 125	2. 92	3. 17	_				
© FREESCALE SEMICONDUCTOR, INC. MECHANICAL OUTLINE PRINT VERSION NOT TO SCA						OT TO SOME			
ALL RIGHTS RESERVED.									
TITLE:				DOCUMENT NO: 98ASA99303D REV:			REV: B		
8 LD SOP, SIDE PORT			CASE NUMBER: 1369-01 24 MAY 2005				24 MAY 2005		
				STANDARD: NON-JEDEC					

PAGE 2 OF 2

CASE 1369-01 ISSUE B SMALL OUTLINE PACKAGE

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

http://www.freescale.com/support

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH Technical Information Center Schatzbogen 7 81829 Muenchen, Germany +44 1296 380 456 (English) +46 8 52200080 (English) +49 89 92103 559 (German) +33 1 69 35 48 48 (French) www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd. Headquarters ARCO Tower 15F 1-8-1, Shimo-Meguro, Meguro-ku, Tokyo 153-0064 Japan 0120 191014 or +81 3 5437 9125 support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd. Technical Information Center 2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale[™] and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2009. All rights reserved.

